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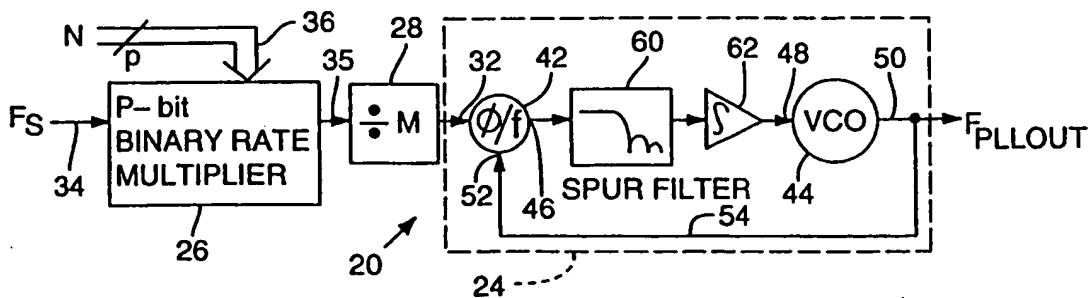
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(54) Phased locked loop synthesizer using a digital rate multiplier reference circuit.

(55) A phase locked loop synthesizer (20) for generating a digitally programmable, continuous wave signal comprises a rate multiplier (26) and divider (28) connected in a reference signal path to a phase detector (42). The rate multiplier and divider generate a reference signal which is programmable to any of a set of regularly spaced frequencies having exact decimal representations. The divider limits the

peak-to-peak phase deviation of the rate multiplier. The phase detector locks a synthesized signal generated by a variable frequency oscillator (44) to the phase of the programmed reference signal. A spur filter (60) connected to the phase detector output (46) reduces spurious frequencies in the phase detector output.

FIG. 1



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EP 95 30 0129

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	US-A-4 965 533 (GILMORE) 23 October 1990 * column 2, line 30 - line 48 * * column 5, line 14 - column 8, line 54; figure 2 *	1,2	H03L7/197 H03L7/183
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Y	---		
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Y	RADIO AND ELECTRONIC ENGINEER, vol. 48, no. 3, March 1978 LONDON GB, pages 127-132, L. K. REGENBOGEN 'A LOOSE-LOCKED OSCILLATOR' * the whole document *	1,2	
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The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	13 September 1995	Balbinot, H	
CATEGORY OF CITED DOCUMENTS			
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THE HAGUE	13 September 1995	Balbinot, H	
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